Remarks/Arguments:

Claims 1-19 are pending and stand rejected.

By this Amendment, claims 1, 2, 9, 11-12, 14 and 16-19 are amended and new claim 19 20 1s added. No new matter is presented by the claim amendments. Support for the claim amendments can be found throughout the original specification and, for example, in the original specification at paragraphs [0024] - [0027].

Claim Objections

In the Office Action, at item 3, claims 9, 12, 14, 16 and 17 are objected to because of informalities therein.

Applicants have amended these claims as suggested by the Examiner.

Reconsideration is respectfully requested.

Rejection of Claim 18 under 35 U.S.C. §112, second paragraph

In the Office Action, at item 4, claim 18 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Claim 18 has been amended to overcome this rejection.

Reconsideration is respectfully requested.

Rejection of Claims 1-3, 5-6, 9, 11-12 and 14-19 under 35 U.S.C. §102(b)

In the Office Action, at item 5, claims 1-3, 5-6, 9, 11-12 and 14-19 are rejected under 35 U.S.C. §102(b) as being anticipated by Gowda et al. (U.S. Patent No.: 5,877,715, hereafter referred to as Gowda).

Reconsideration is respectfully requested.

Claim 1

Claim 1 is directed to a pixel-capture circuit, and recites "a reset node carrying a reset signal that is operable to couple the row node to the pixel node during the reset period, wherein the row signal changes between a predetermined voltage level during at least one portion of the reset period and sets the pixel node to the predetermined signal level such that the row node is coupled to the pixel node during the reset period." That is, the row node (carrying the row signal which changes between predetermined voltage levels) is coupled to the pixel node during the reset period.

Gowda Reference

Gowda discloses a gate node of transistor 22 which the Examiner corresponds to the row node of claim 1 and the cathode node of photodiode 26 which the Examiner corresponds to the pixel node of claim 1. Applicants submit that the gate of reset transistor 21 corresponds to the

reset node. Contrary to the recitation in claim 1, the reset node (i.e., gate of reset transitor 21) which carries a reset signal is not operable to couple the row node to the pixel node during the reset period. This is because, the reset node is not positioned electrically between the row node and the pixel node. In Gowda, the reset signal carried on the reset node does not control coupling to the pixel node, instead transistors 22 of Gowda controls such coupling.

Accordingly, it is submitted that claim 1 patentably distinguishes over Gowda for at least the above mentioned reasons.

Claims 11 and 14

Claims 11 and 14, which include similar but not identical features to those of claim 1, are submitted to patentably distinguish over Gowda for at least similar reasons to those of claim 1.

Claims 2-3, 5-6, 12, 15 and 19

Claims 2-3, 5-6, 12 and 15, which include all of the limitations of claim 1, 11 or 14 are submitted to patentably distinguish over Gowda for at least the same reasons as their respective independent claims.

Claim 9

Claim 9 is directed to a pixel capture circuit and recites "a second transistor having a control node, a first drive node, a second drive node, the control node of the second transistor connected to a row node, the first drive node of the second transistor connected to the second drive node of the first transistor, the second drive node of the second transistor directly connected to a column node."

Gowda Reference

In the Office Action, the Examiner corresponds the second transistor recited in claim 1 to transistor 22 of Gowda. It is clear from, for example, FIG. 4 that transistor 22 of Gowda is not directly connected to column node (which the Examiner corresponds to line 15j). This is because, source follower FET 23 is provided between transistor 22 and column node 15j.

Accordingly, it is submitted that claim 9 patentably distinguishes over Gowda for at least the above mentioned reasons.

Claim 16

Claim 16 is directed to a method and recites "the resetting of the signal level ... includes connecting the first control node to the pixel node via a switching device." As previously mentioned, the Examiner corresponds the first control node recited in claim 16 to gate node of row transistor 22 of Gowda and the pixel node recited in claim 16 to the cathode node of photodiode 26 of Gowda. In Gowda, however, the first control node (i.e., row select) having a

first control signal that changes between predetermined levels is not connected to the cathode node of photodiode 26, but instead controls the connection of reference node 25 to photodiode 26.

Accordingly claim 16 patentably distinguishes over Gowda for at least the above mentioned reasons.

Claims 17 and 18

Claims 17 and 18, which include all of the limitations of claim 16, are submitted to patentably distinguish over Gowda for at least the same reasons as claim 16.

Rejection of Claims 4, 7-8 and 13 under 35 U.S.C. §103(a)

In the Office Action, at item 6, claims 4, 7-8 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Gowda in view of Sasaki (U.S. Patent No. 6,150,676).

Reconsideration is respectfully requested.

Claims 4, 7-8 and 13, which include all of the limitations of claim 1 or 11, are submitted to patentably distinguish over Gowda for at least the same reasons as their respective independent claims.

The addition of Sasaki does not overcome the deficiencies of Gowda. This is because, for example, with regard to FIG. 3 of Sasaki, reset transistor Q5 carrying a reset signal is not operable to couple the row node to the pixel node during the reset period, as required by claim 1. Instead, the photodiode D1 is controlled to couple to node N1 via read transistor Q2 and, more particularly, is not controlled to couple via reset transistor Q5.

Accordingly, it is submitted that claims 4, 7-8 and 13 patentably distinguish over Gowda in view of Sasaki for at least the same reasons as their respective base claims.

Rejection of Claim 10 under 35 U.S.C. §103(a)

In the Office Action, at item 7, claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over Gowda in view of Fossum et al. (U.S. Patent No. 5,949,483, hereafter referred to as Fossum).

Reconsideration is respectfully requested.

Claim 10, which includes all of the limitations of claim 9, is submitted to patentably distinguish over Gowda for at least the same reasons as claim 9.

The addition of Fossum does not overcome the deficiencies of Gowda. This is because, Fossum, for example, does not disclose or suggest the structure recited in claim 9. More particularly, Fossum does not disclose or suggest the row node defined in claim 9 and, furthermore, the connection of the control node of the second transistor and the first drive node of the third transistor to the row node.

Accordingly, it is submitted that claim 10 patentably distinguishes over Gowda in view of Fossum for at least the above-mentioned reasons.

New Claim 20

New claim 20, which include all of the limitations of claim 1, is submitted to patentably distinguish over the cited art for at least the same reasons as claim 1.

New claim 20 includes a patentable distinction beyond that of claim 19, namely: "a further transistor coupled between the pixel capture device and the row selection transistor, the row selection transistor being disposed between the further transistor and the column trace."

Consideration and approval is respectfully requested.

Conclusion

In view of the claim amendments, new claim and remarks, Applicants submit the application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,

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